**ECE 429 Lab 4**

**Gate Delay and Power**

**David Cho**

**A20384999**

**02/20/2020**

**Introduction**

The objective of this lab is to draw and measure schematic of a 2-input NAND gate. HSPICE will be used to study how the transistor sizes, load capacitances, and input transitions will affect the gate delay and power.

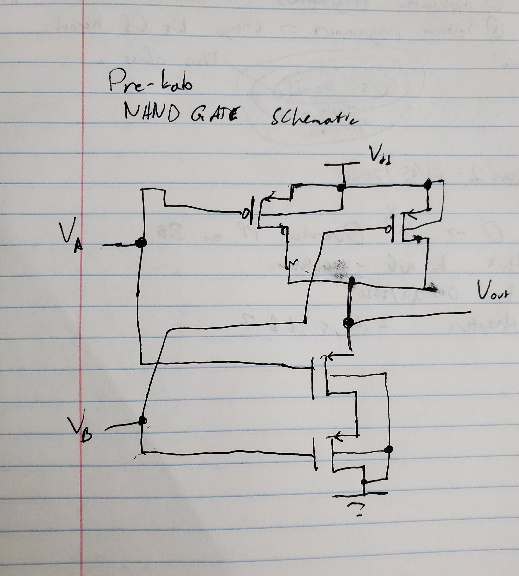
**Theory/Pre-Lab**

While CosmosScope can measure the delays in designs, it is more convenient to perform measurements within a SPICE netlist so that the delays can be directly obtained from the output of the HSPICE simulation. SPICE statements can be added to measure the rising and falling delays in a design. The same can be done to measure the average power consumption of the design. This lab will use HSPICE to take measurements of delays in a NAND gate.

This lab will take measurements for different load capacitances, transistor widths, and signal transitions.

Prior to the lab, a sketch of the NAND gate schematic was drawn.

**Figure 1: Pre-lab NAND schematic**

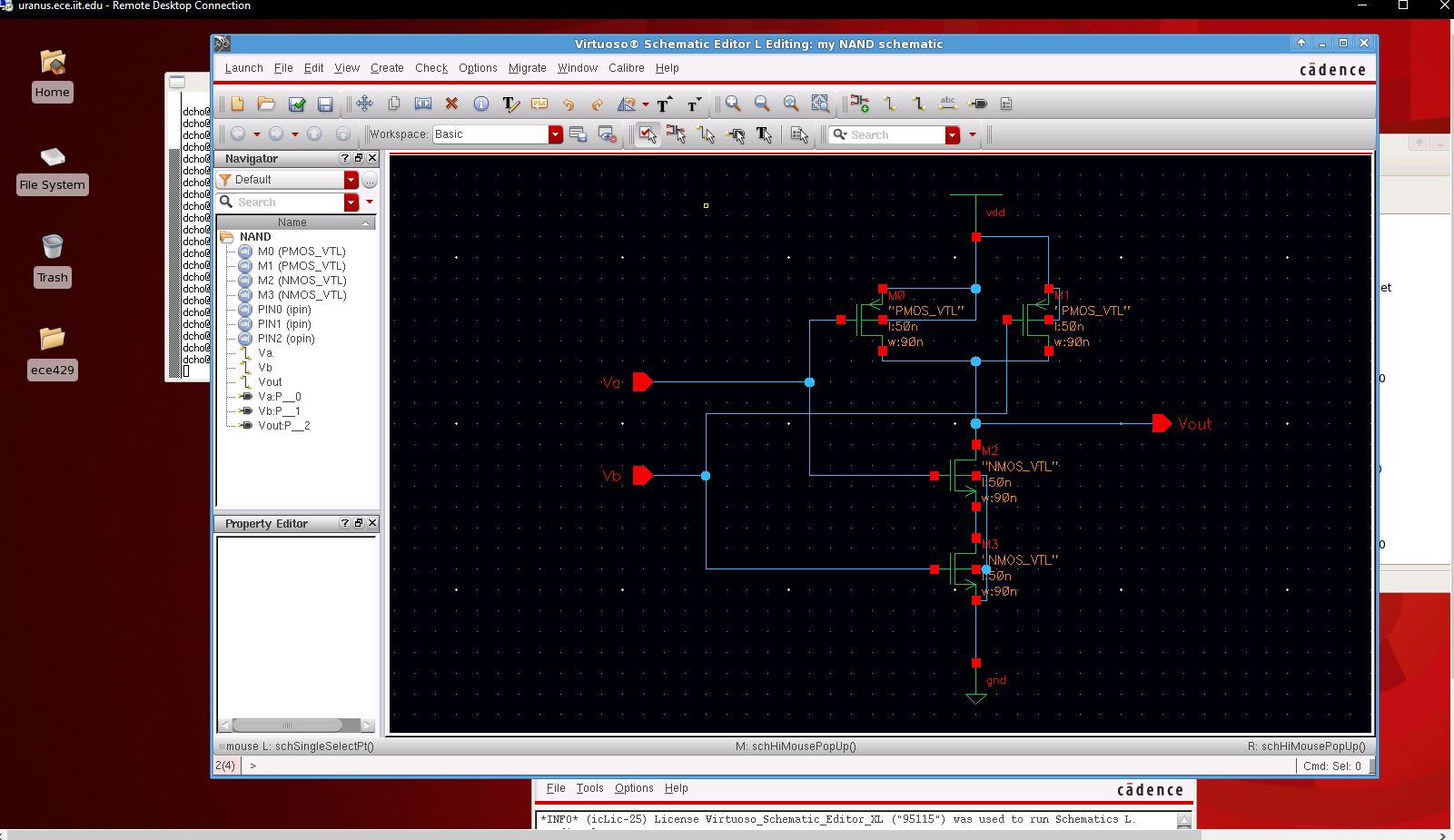
****

The top two transistors are the location of the PMOS, while the bottom two are the NMOS transistors. It is hypothesized that the input transitions that would lead to the maximum rising or falling delays would be the transition of 10 rising to 11 and 11 falling back to 00, respectively.

**Implementation**

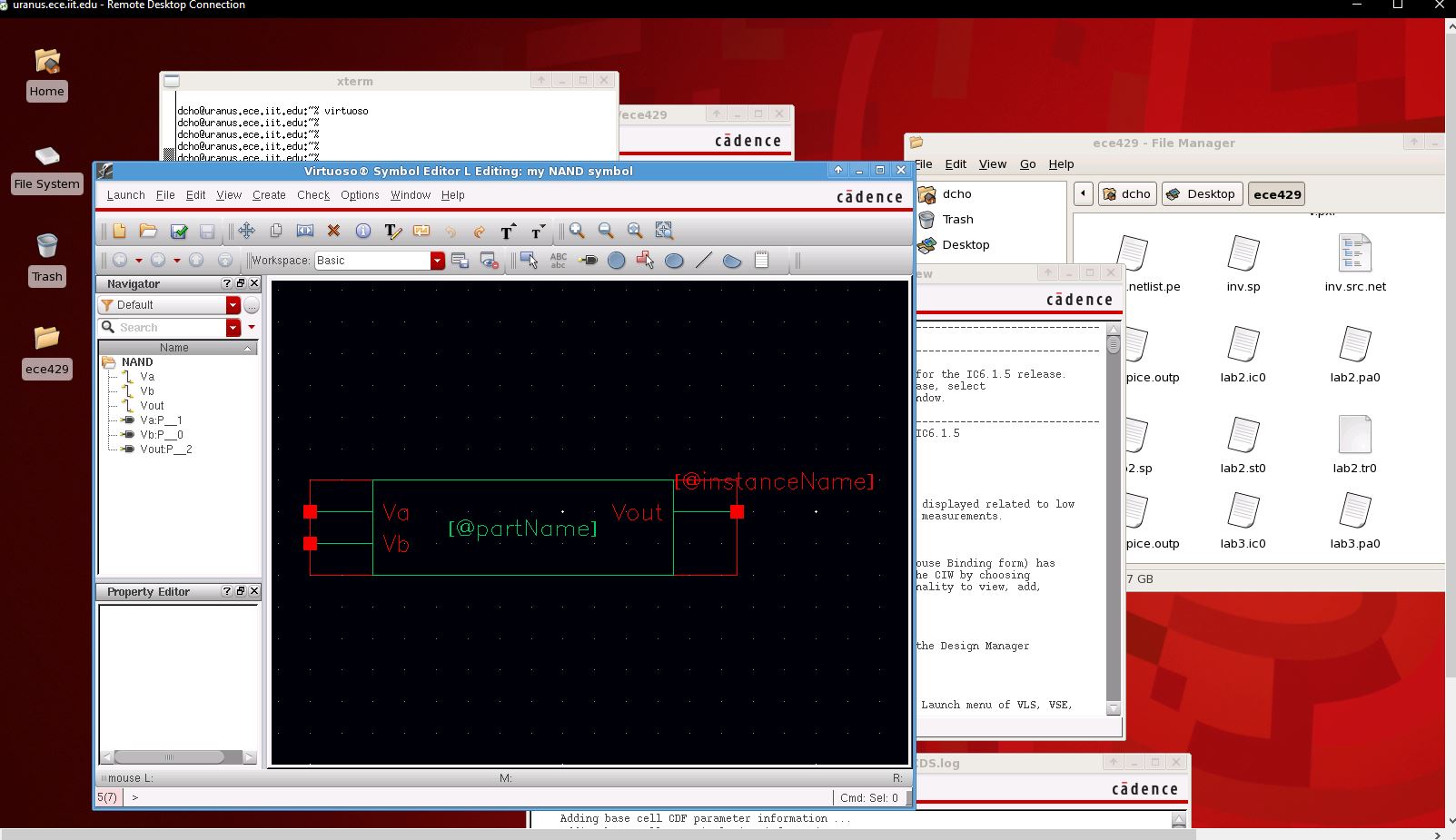
From the sketch in the pre-lab, the following schematic for a NAND gate was created in Virtuoso.

**Figure 2: NAND Gate Schematic**

****

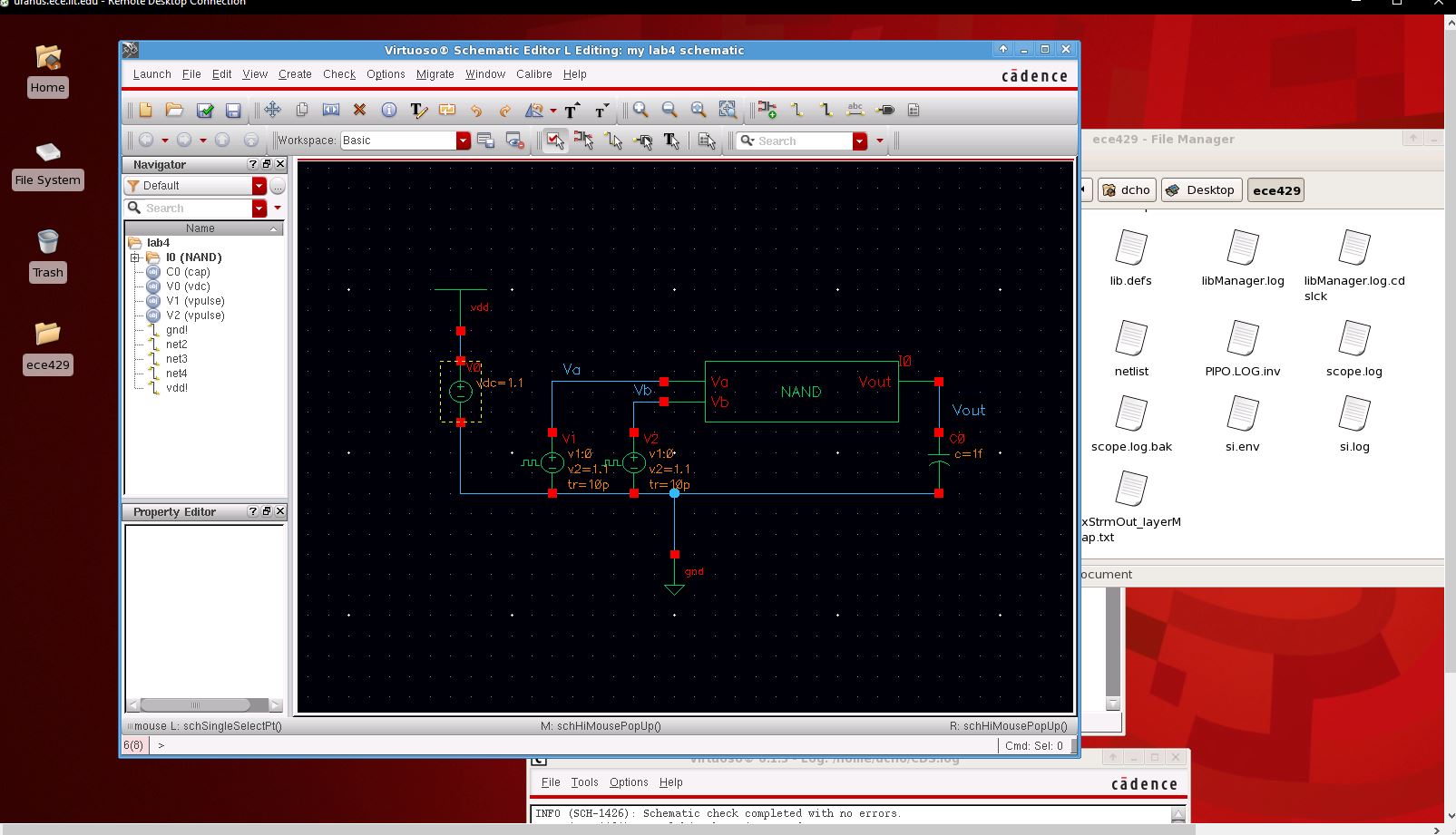
The symbol was then created from the schematic, for use in a test circuit.

**Figure 3: NAND Gate Symbol**



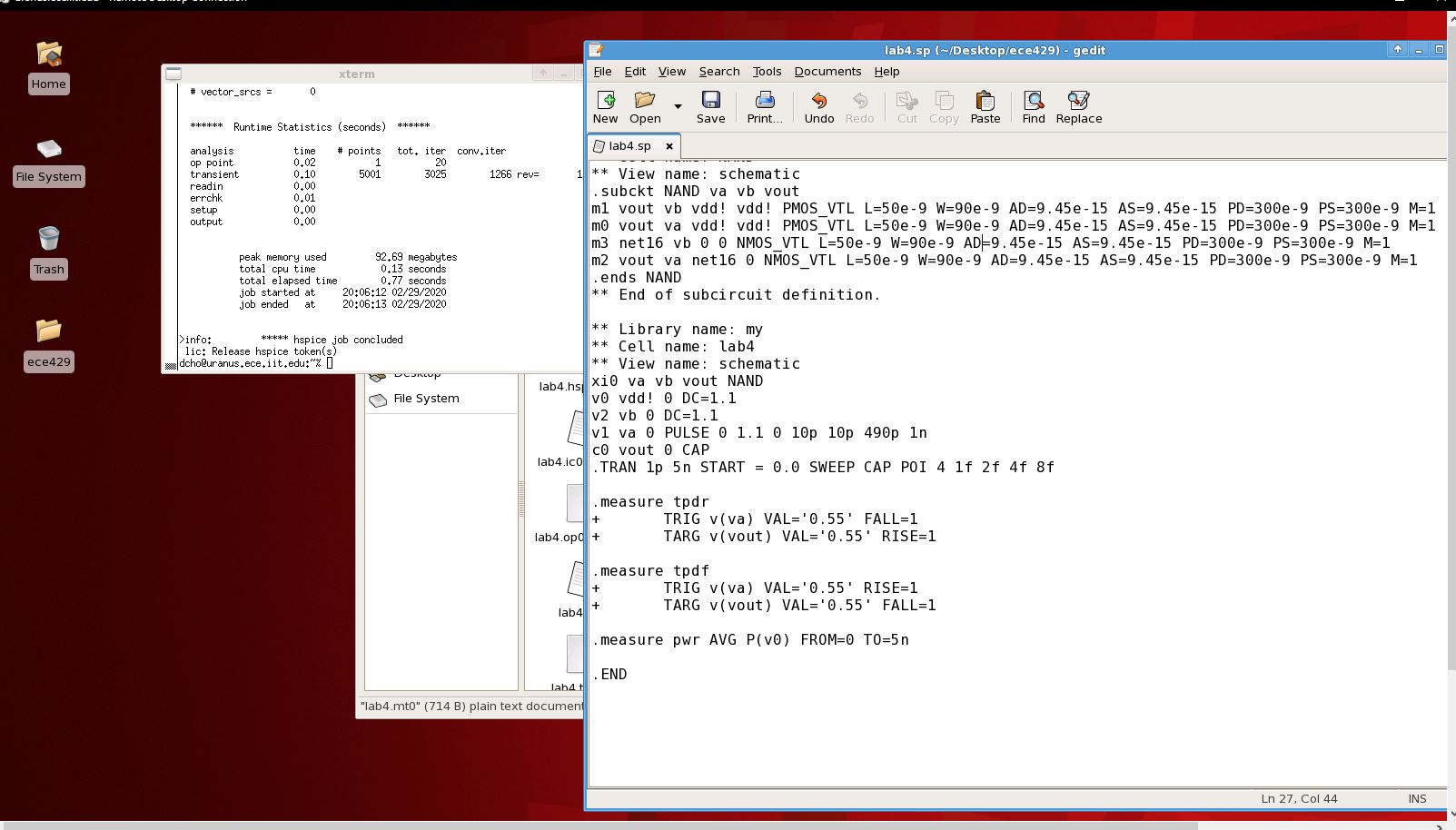
The test circuit below was used to test the NAND gate in HSPICE.

**Figure 4: NAND Gate Test Circuit**

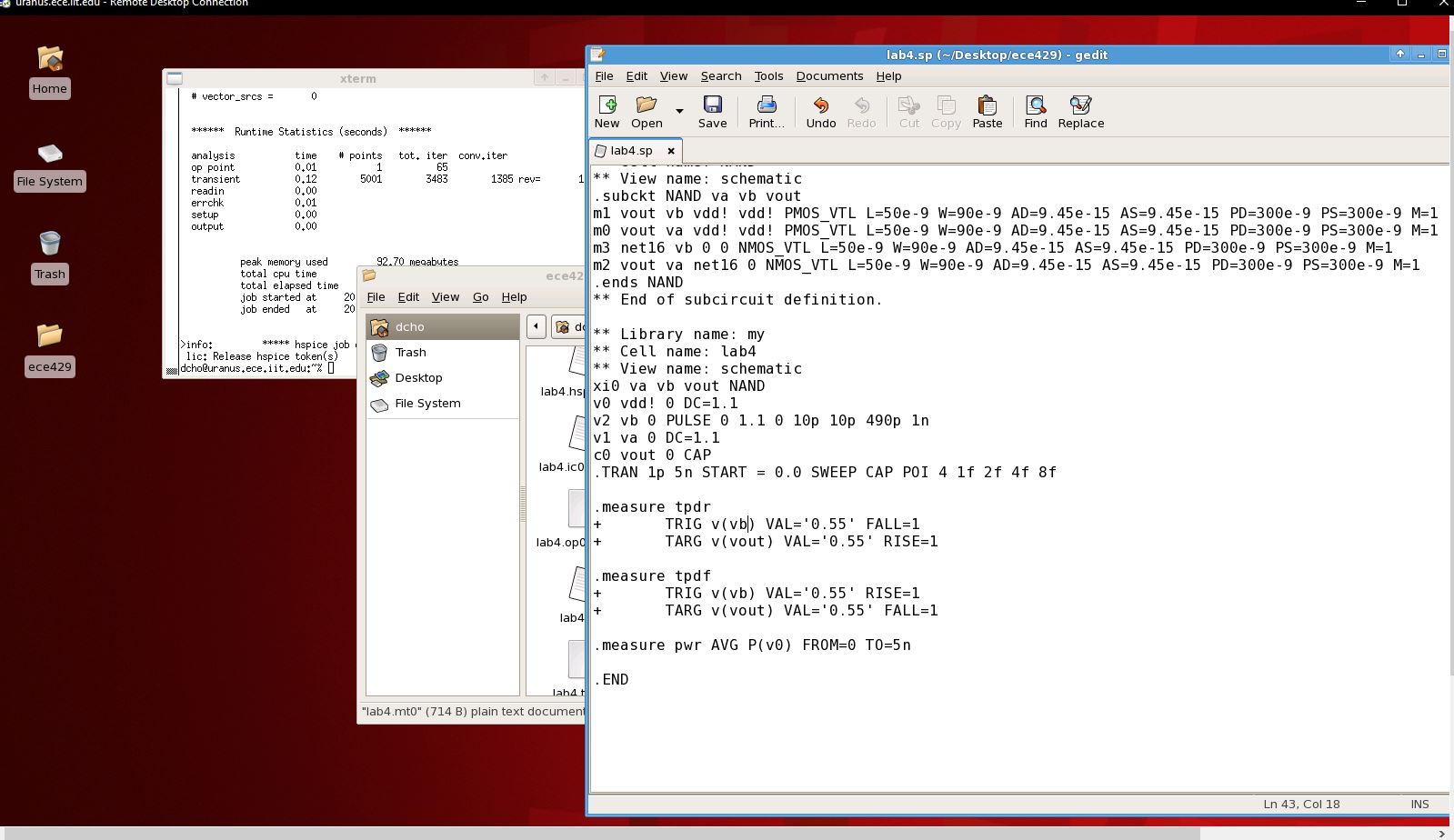


From this test circuit, a lab4.sp file was created. This file is what is used by HSPICE to simulate the circuit. The modified netlists can be seen below. The three netlists depict what the netlists look like when testing the 3 different signal transitions. The modifications to measure the rising delays, falling delays, and power can be seen as well.

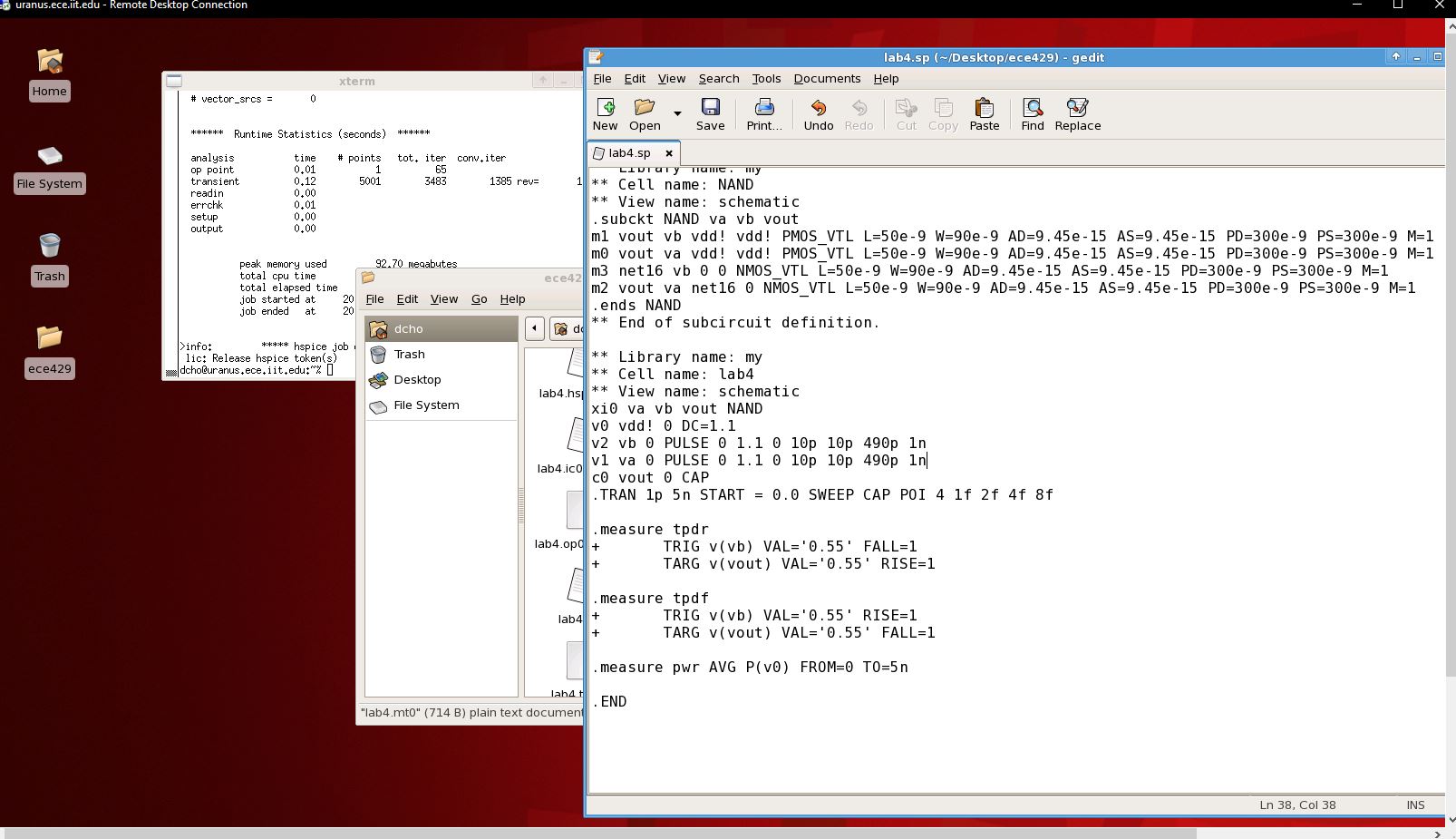
**Figure 5: Transition 01🡪11, 11🡪 01 Netlist**

****

**Figure 6: Transition 10🡪11, 11🡪 10 Netlist**

****

**Figure 7: Transition 00🡪11, 11🡪 00 Netlist**

****

The netlist modification for each transition is the same between the different transistor widths, so it would be redundant to display those here.

Due to the number of screenshots, the mt0 files (the files that hold the measurements) are displayed in the appendix as Figures 11-19. Figures 8-10 are tables that were created from these measurement files. The rising/falling delays were chosen from the three transitions, and for each load capacitance, the maximum delay was chosen. The corresponding transition can be seen. The power consumption is the average consumption between the three transitions.

**Figure 8: 90nm**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| W=90nm  L=50nm | Load Capacitance (F) | | | |
| 1f | 2f | 4f | 8f |
| Rising Propagation Delay (s) | 1.595e-11  (10🡪11) | 2.378e-11  (10🡪11) | 3.869e-11  (10🡪11) | 6.897e-11  (10🡪11) |
| Falling Propagation Delay (s) | 1.613e-11  (11🡪10) | 2.483e-11  (11🡪10) | 4.151e-11  (11🡪10) | 7.347e-11  (11🡪00) |
| Average Power Consumption (W) | 2.070e-6 | 3.295e-6 | 5.711e-6 | 1.056e-5 |

**Figure 9: 180nm**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| W=180nm  L=50nm | Load Capacitance (F) | | | |
| 1f | 2f | 4f | 8f |
| Rising Propagation Delay (s) | 1.023e-11  (10🡪11) | 1.389e-11 (10🡪11) | 2.125e-11  (10🡪11) | 3.596e-11  (10🡪11) |
| Falling Propagation Delay (s) | 1.024e-11  (11🡪00) | 1.437e-11 (11🡪00) | 2.237e-11  (11🡪00) | 3.837e-11 (11🡪00) |
| Average Power Consumption (W) | 2.549e-6 | 3.775e-6 | 6.228e-6 | 1.108e-5 |

**Figure 10: 270nm**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| W=270nm  L=50nm | Load Capacitance (F) | | | |
| 1f | 2f | 4f | 8f |
| Rising Propagation Delay (s) | 8.425e-12  (10🡪11) | 1.081e-11  (10🡪11) | 1.564e-11  (10🡪11) | 2.527e-11  (10🡪11) |
| Falling Propagation Delay (s) | 8.638e-12  (11🡪00) | 1.119e-11  (11🡪00) | 1.643e-11  (11🡪00) | 2.683e-11  (11🡪00) |
| Average Power Consumption (W) | 3.038e-6 | 4.231e-6 | 6.695e-6 | 1.158e-5 |

**Deliverable Questions**

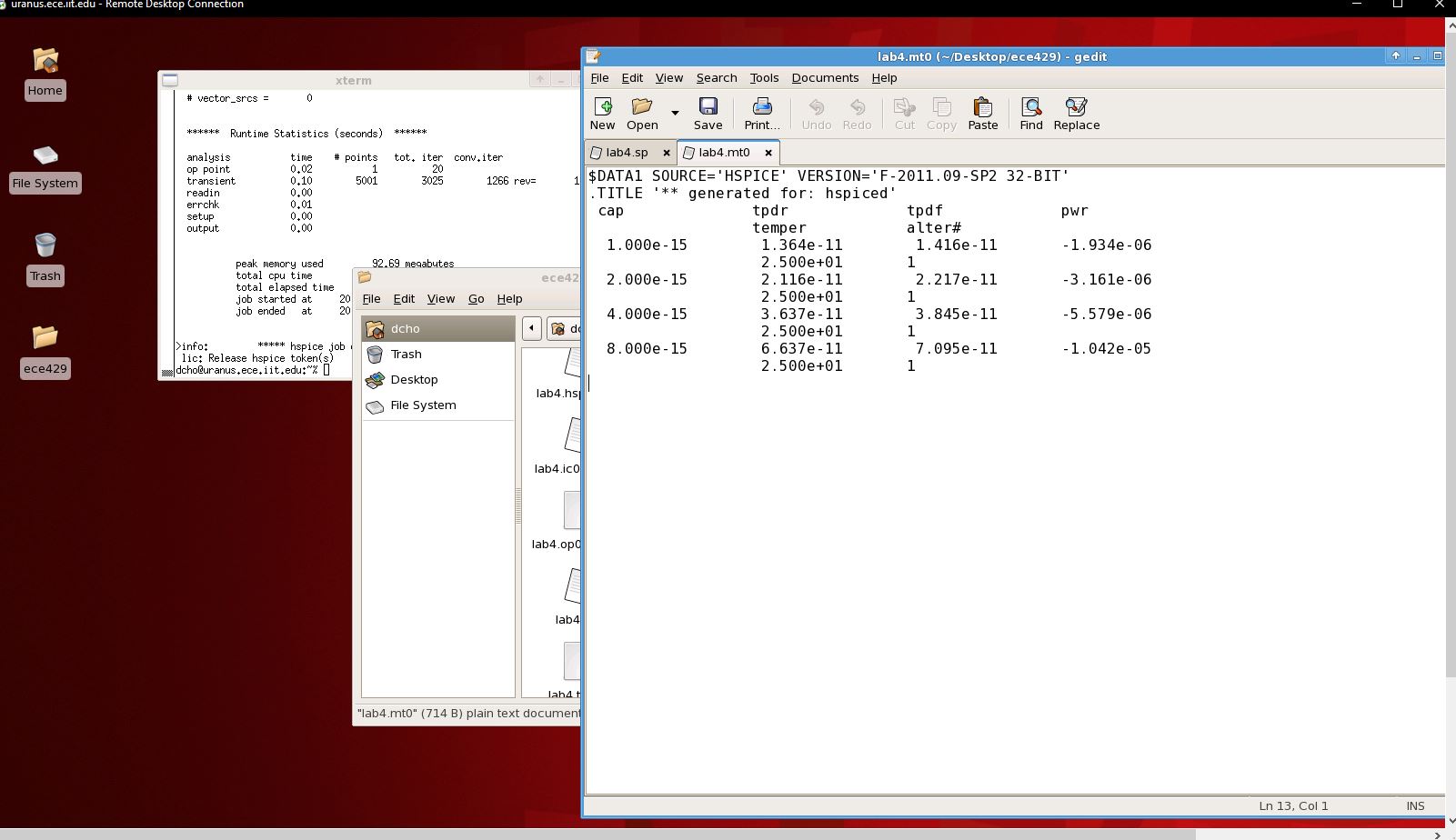
1. I expect that the transition from 10 🡪 11 will have the maximum rising delay, and 00🡪11 has the maximum falling delay because the maximum rising delay would be when the n-transistor closer to the output becomes a 1 signal. The maximum falling delay would be when both of the p-type transistors become a 0 signal. As can be seen from the results of the experiment, the results largely match the expectations. For the 90nm width experiment, 3 of the 4 maximum falling delays are the transition from 11🡪10. Even so, the difference in delays are minimal. Aside from this, the results are as expected.
2. Yes, the relationship between transistor sizes, load capacitances, and propagation delays follow the linear delay model, d = gh + p. Given a linear graph figure of this NAND gate, where the graph is Delay vs Capacitance, the parasitic delay could be obtained when the Capacitance is 0. The slope of the graph would be the Logical Effort.
3. Power consumption increases both as transistor sizes go up, and as load capacitances go up.
4. Dynamic power is the power that is measured in this lab. The driving force of power consumption is dynamic power, and since we are measuring the power consumption, it is logical to conclude that this lab measures Dynamic power.

**Conclusion**

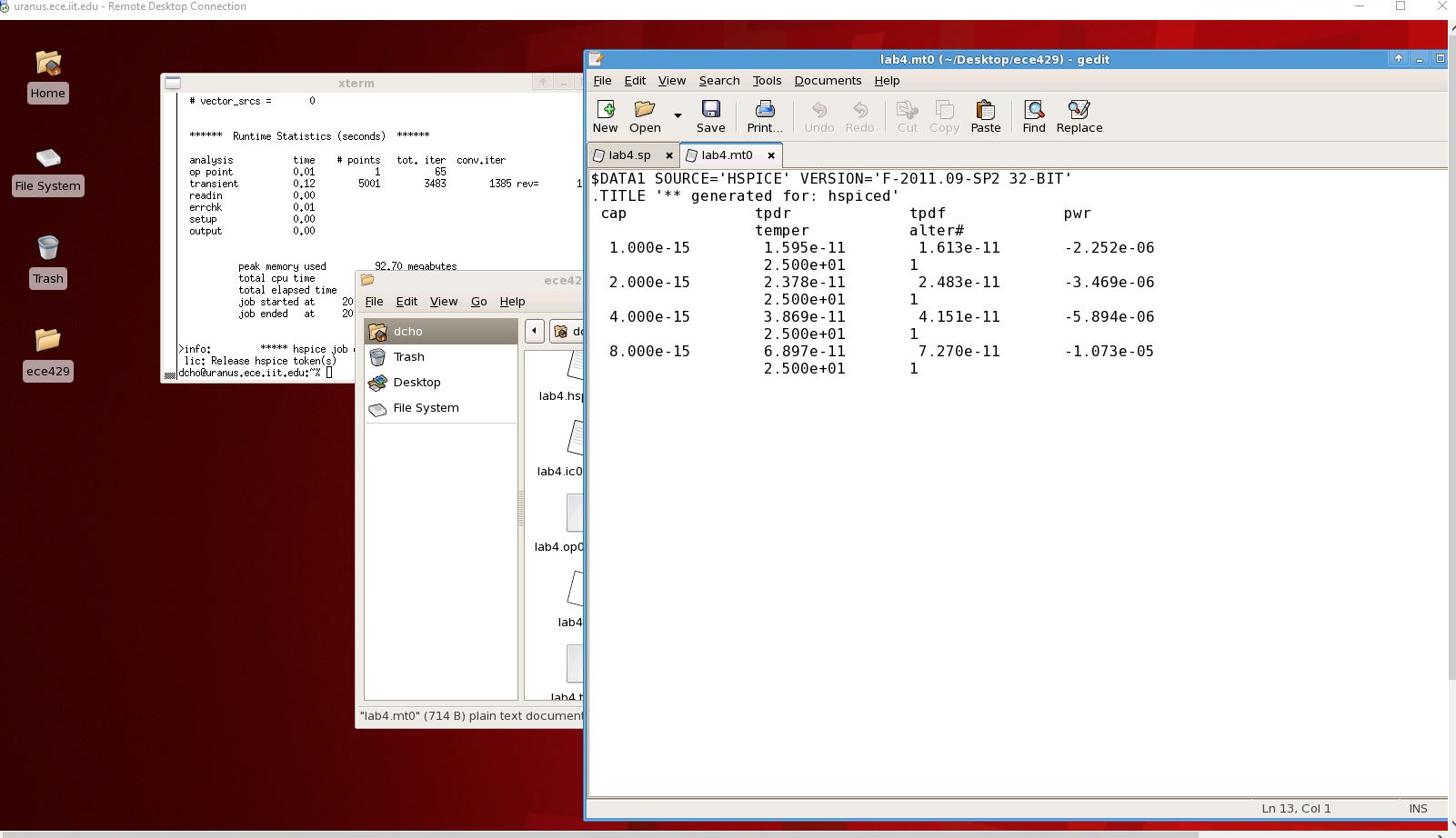
In conclusion, this lab was successful. The 2 input NAND gate was successfully created and simulated. Most of the results were as expected, and any errors and difficulties while designing and testing were quickly figured out. This lab also made me more confident in the use of Virtuoso and HSPICE. Although I am satisfied with the results, it is possible that there were errors while doing the lab. For example, something in the netlist may have been changed accidentally while changing the netlist. This makes it possible that there are errors in the measurement.

**Appendix**

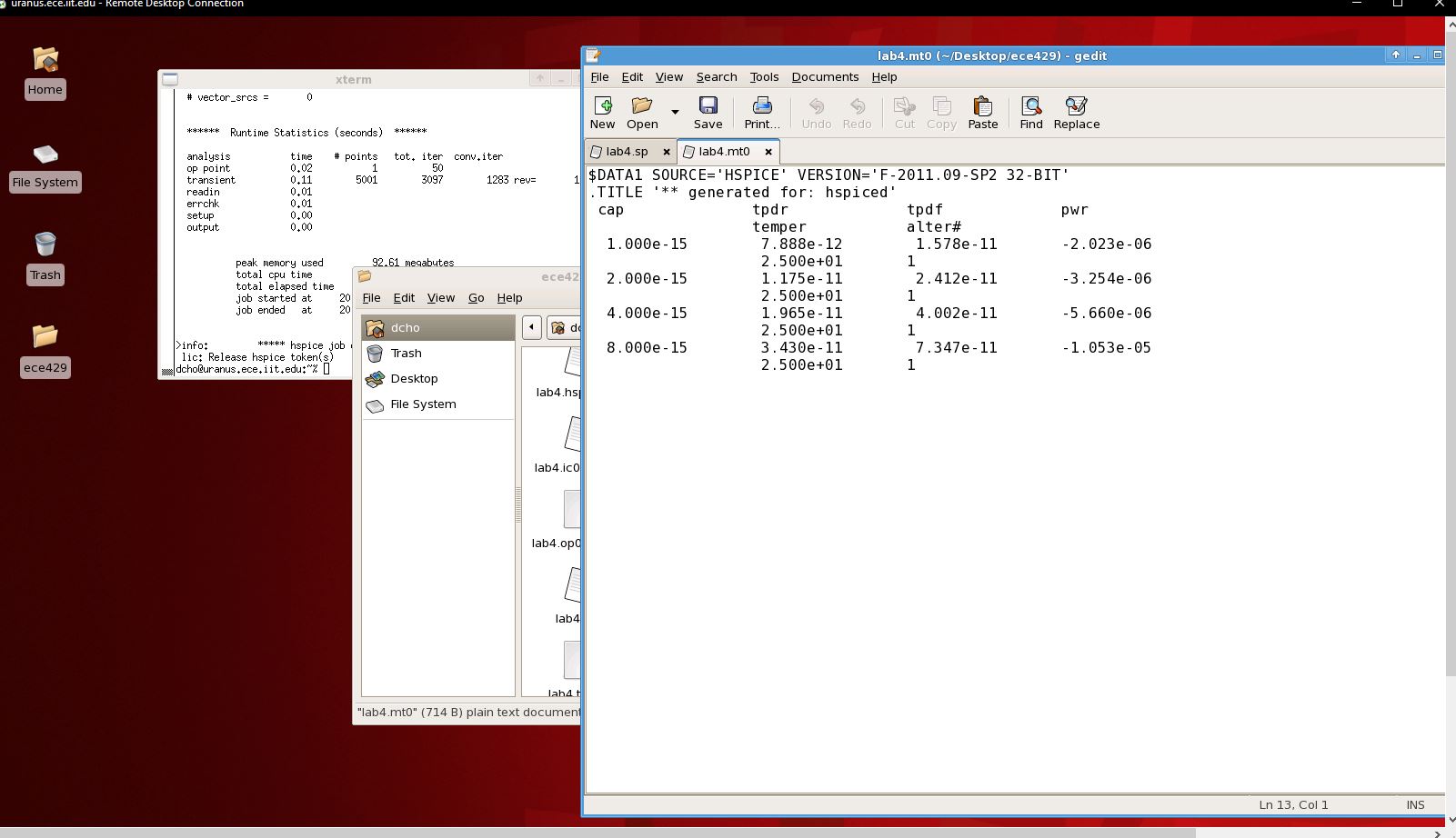
**Figure 11: Width 90nm, 01🡪11, 11🡪01**

****

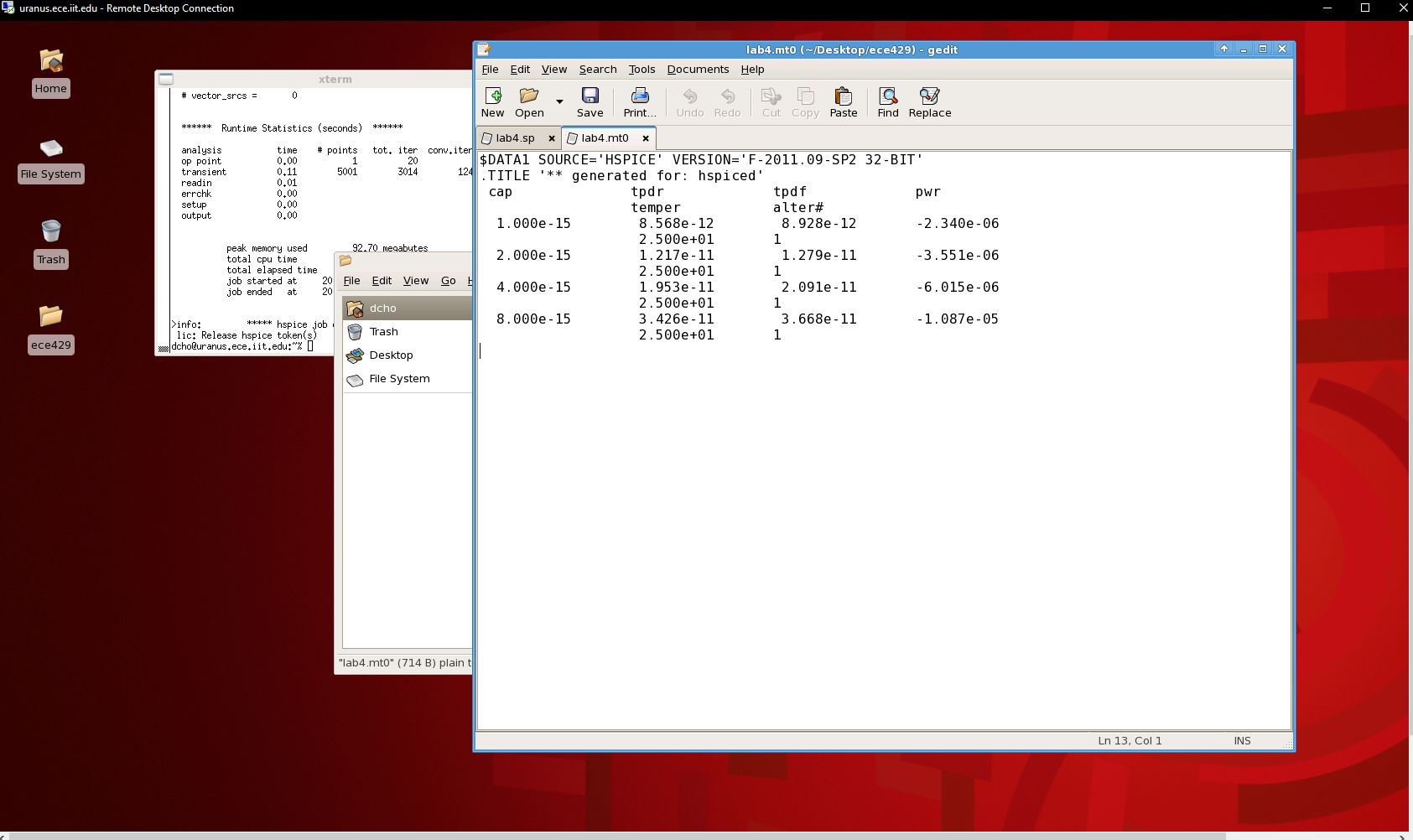
**Figure 12: Width 90nm, 10🡪11, 11🡪10**

****

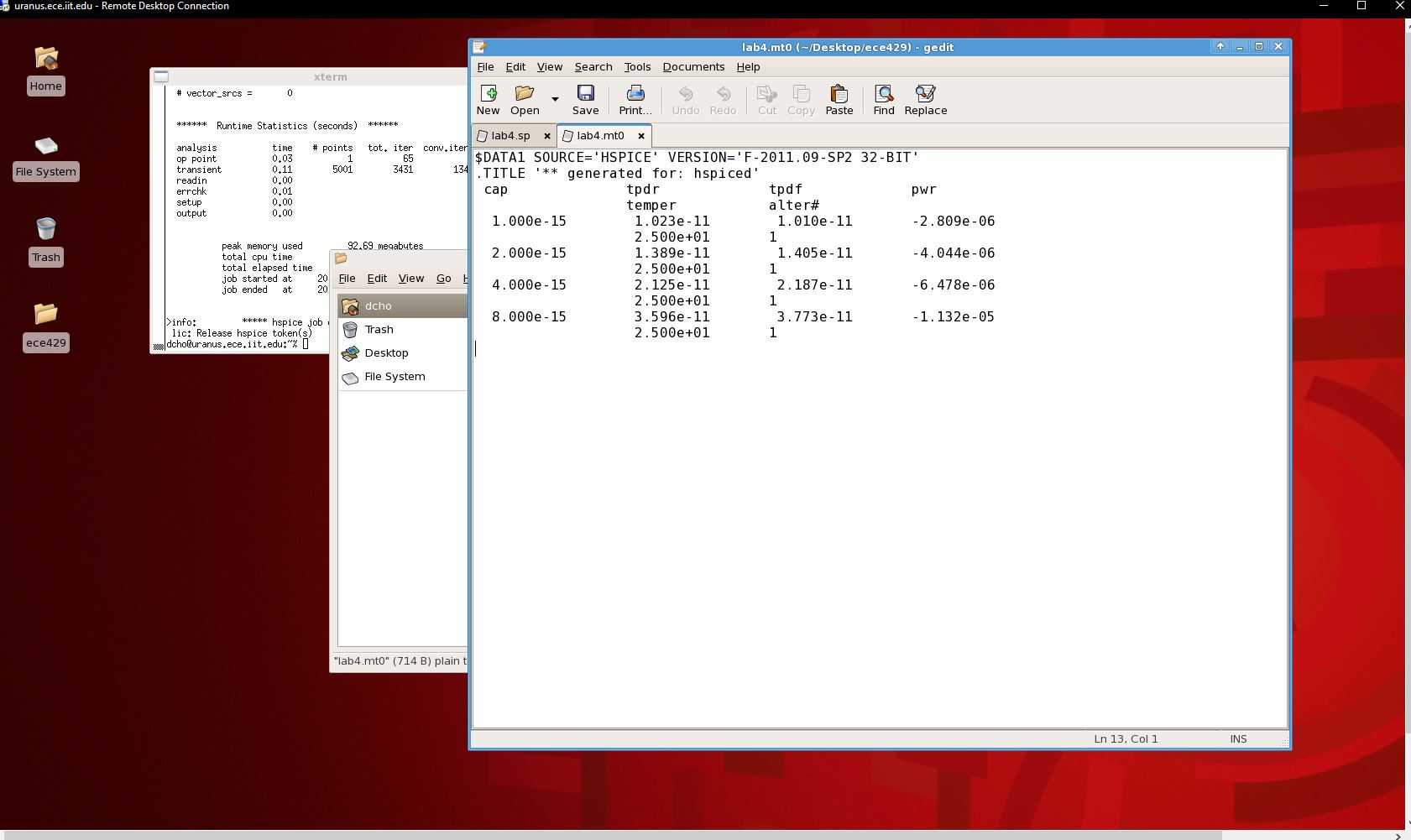
**Figure 13: Width 90nm, 00🡪11, 11🡪00**

****

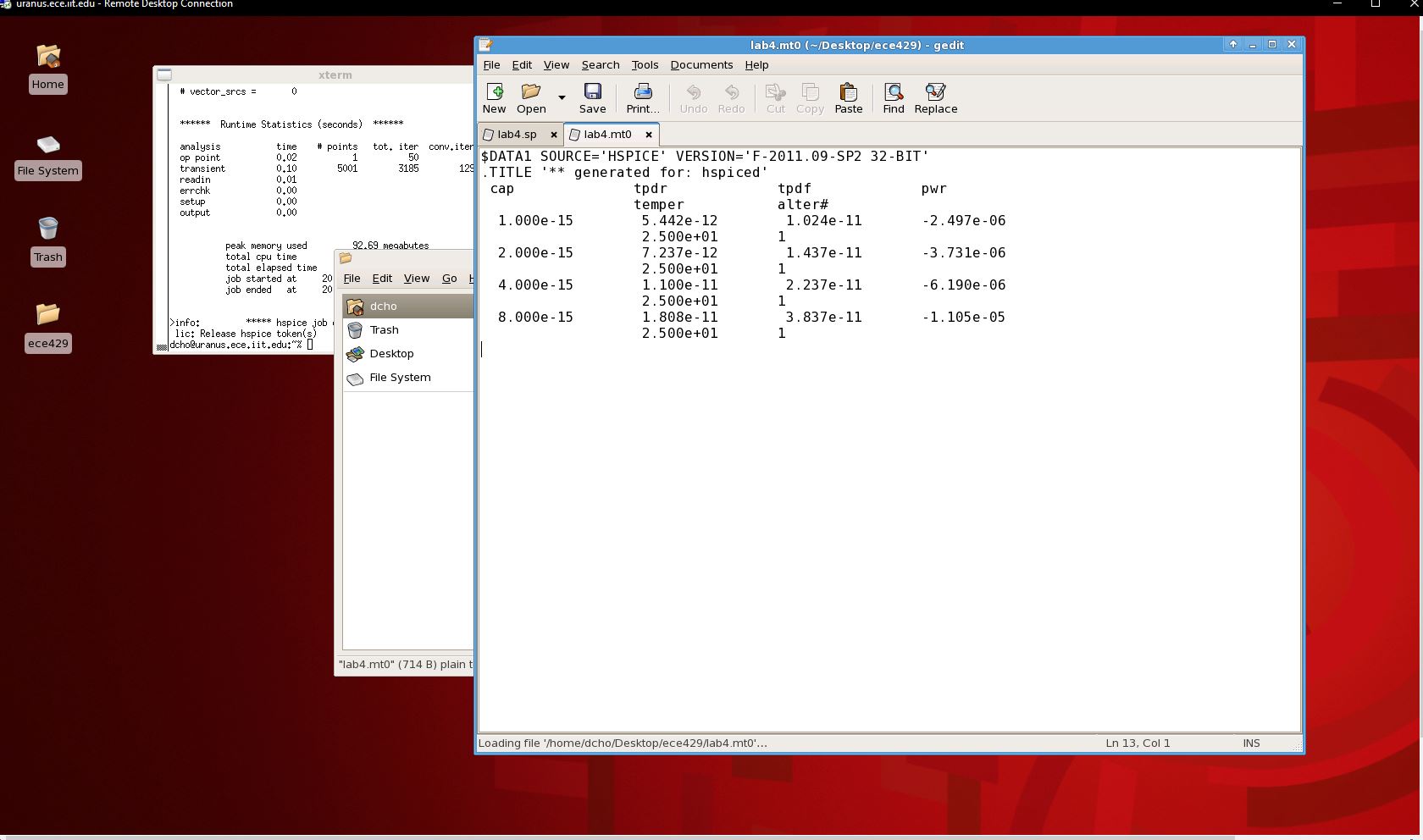
**Figure 14: Width 180nm, 01🡪11, 11🡪01**

****

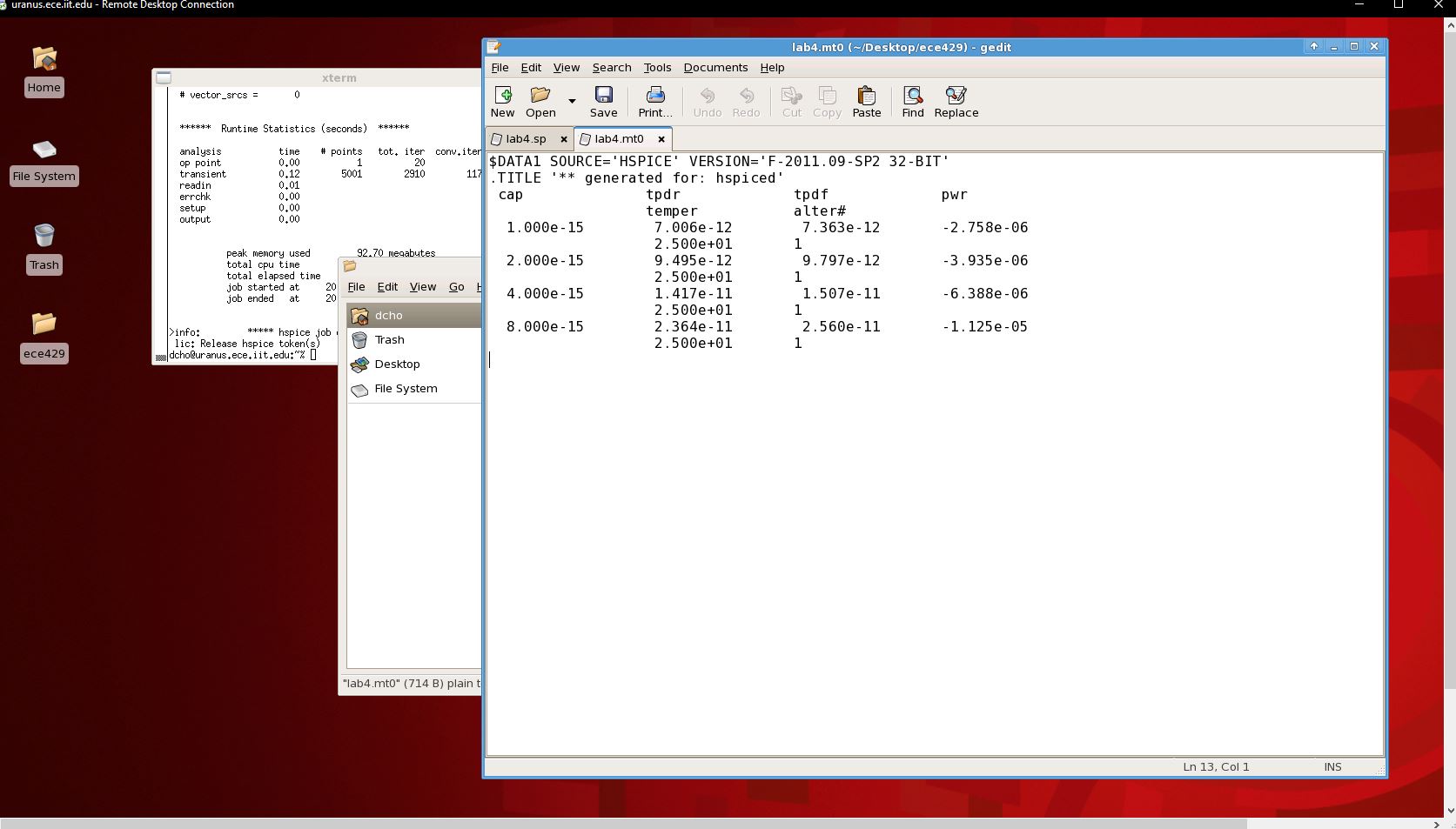
**Figure 15: Width 180nm, 10🡪11, 11🡪10**

****

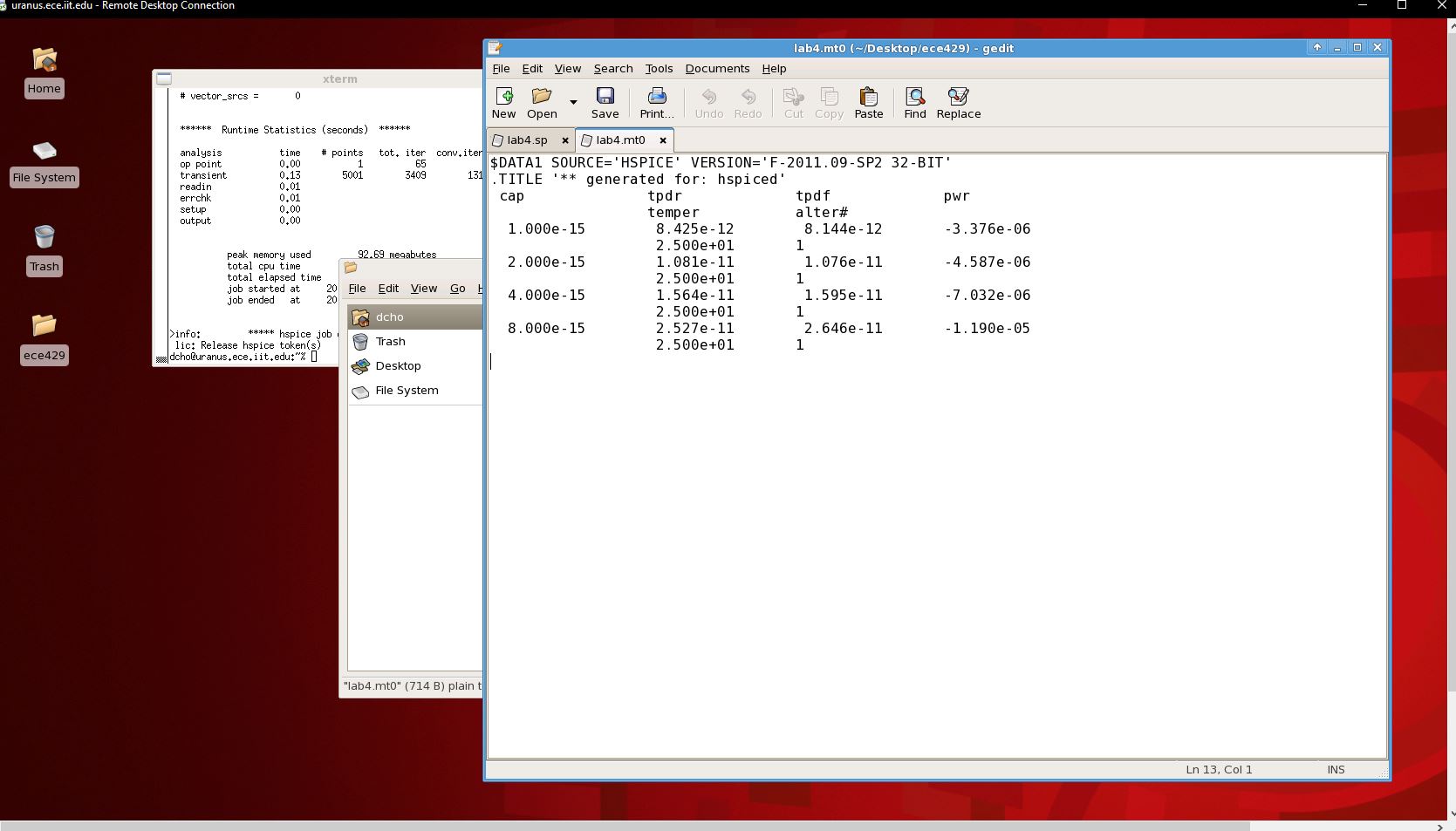
**Figure 16: Width 180nm, 00🡪11, 11🡪00**



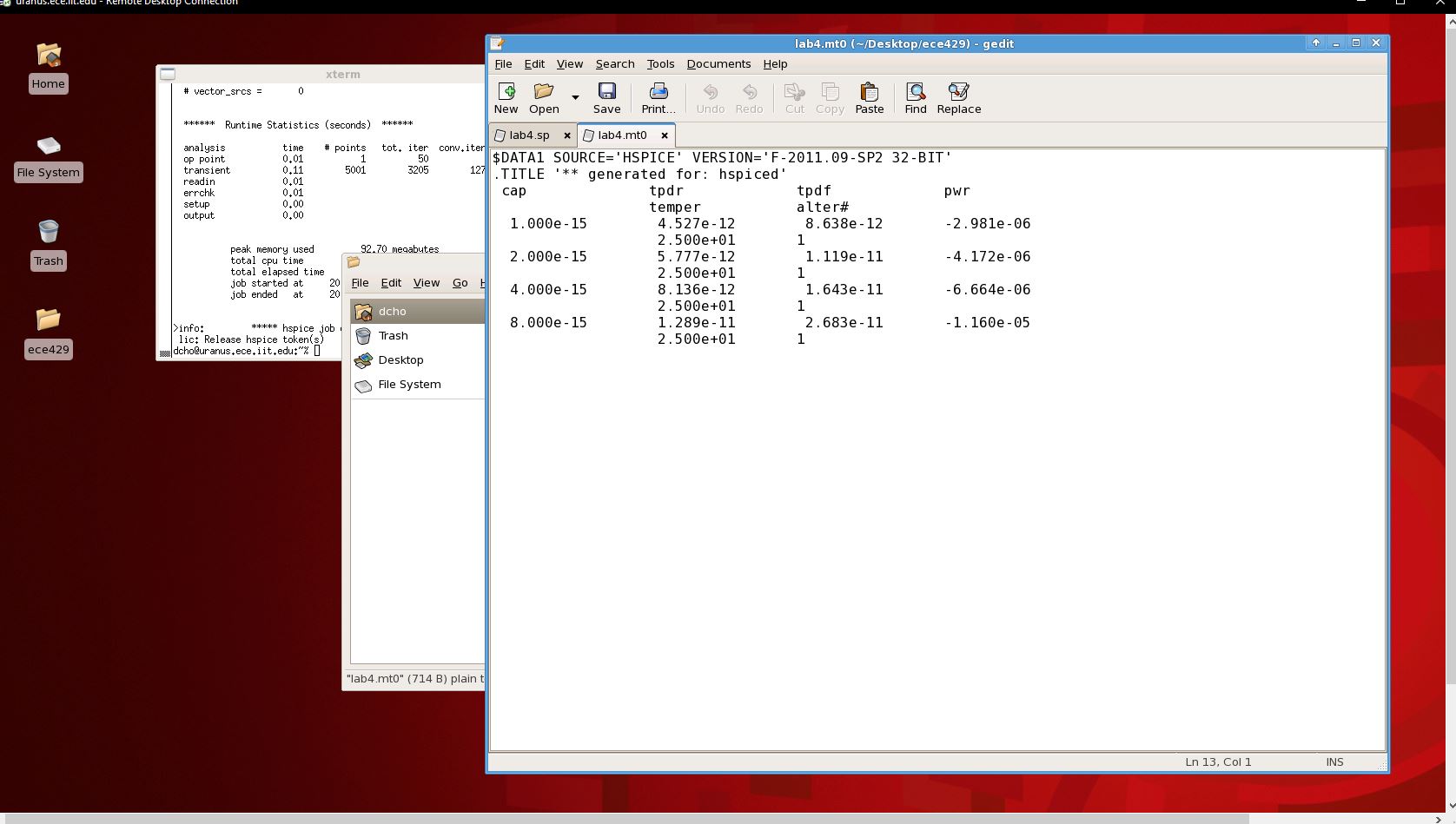
**Figure 17: Width 270nm, 01🡪11, 11🡪01**



**Figure 18: Width 270nm, 10🡪11, 11🡪10**



**Figure 19: Width 270nm, 00🡪11, 11🡪00**

****